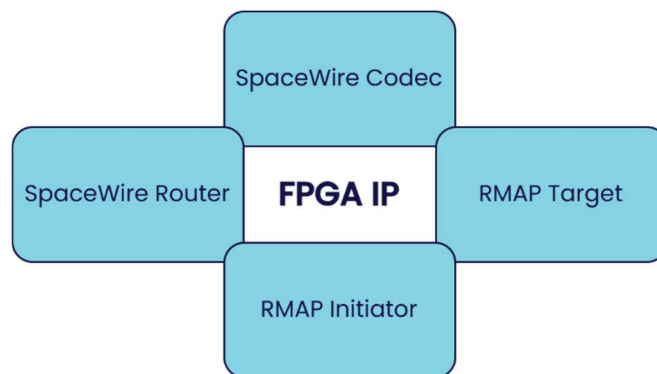


Open-Source FPGA IP Product Brief



Product Overview

4Links offer a range of open-source FPGA IP under a permissive BSD license. Currently, the following IP are available on request:

- SpaceWire Codec
- SpaceWire Router
- RMAP Target
- RMAP Initiator

All are delivered as VHDL source files, with testbenches, example projects, and Vivado build scripts included. All source files are left unencrypted to allow for modification by the end user. Wherever possible, device specific primitives have been avoided, allowing for easy adaptation to any FPGA.

SpaceWire Codec capable
of up to 400Mbps

Complete RMAP
implementation

SpaceWire Router with
support for up to 31 ports

SpaceWire Codec

- Fully compliant to the SpaceWire standard (ECSS-E-ST-50-12C)
- Capable of up-to 400Mbps
- Separate interfaces for data and timecodes
- FPGA vendor agnostic design
- Included example designs targeting Xilinx parts

Example resource usage of a SpaceWire Codec (XCKU040, default synthesis strategy)

LUT	331
FF	385
BRAM	0

RMAP

- Target and Initiator cores provided
- Fully compliant to the RMAP standard (ECSS-E-ST-50-52C)
- Makes use of the 4Links SpaceWire Codec
- Comprehensive simulation library provided alongside a basic testbench

Example resource usage of RMAP cores (XCKU040, default synthesis strategy)

	Target	Initiator
LUT	752	620
FF	765	943
BRAM	0	0

SpaceWire Router

- Configurable up-to 32 routing ports (31 physical, 1 virtual)
- Non-blocking X-bar architecture
- Configurable X-bar width allowing for greater flexibility in core clock rate
- RMAP Configuration via Port 0
- Makes use of the 4Links SpaceWire Codec and RMAP cores
- Example design and testbench included

Example resource usage of a 32 port router at 400Mbps with 2-bit X-bar fabric width (XCKU040, default synthesis strategy)

LUT	27,405
FF	230,881
BRAM	18



Get in touch

To request 4Links Open-Source FPGA IP, please email support@4links.space from your company email address.

For all other enquiries, please contact us at sales@4links.space

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